Low-Cost Capacitance Profiling of a Semiconductor

Contact Information

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Photographs of Apparatus

USB-6009 Implementation:

(myDAQ device is only being used to supply ±15 Volt power to the op-amp circuit)
myDAQ Implementation:
Semiconix Semiconductor STPS20120D Schottky Diode (Mouser PN 511-STPS20120D):
Equipment List

USB-609 Implementation:

1. National Instruments USB-609 DAQ Device
2. Agilent 33210A Function Generator
3. Semiconix Semiconductor STPS20120D Schottky Diode (available from Mouser)
4. 1 nF Capacitor (for Calibration)
5. LF411 Op-Amp and 1 MΩ Resistor
6. Powered Breadboard

myDAQ Implementation:

1. National Instruments myDAQ DAQ Device
2. Semiconix Semiconductor STPS20120D Schottky Diode (available from Mouser)
3. 1 nF Capacitor (for Calibration)
4. Two LF411 Op-Amp, Two 10 kΩ Resistors, 1 MΩ Resistor, 1.5 nF Capacitor
5. Powered Breadboard (Protoboard for NI myDAQ available from Studica)
Low-Cost Capacitance-Voltage Profiling of a Semiconductor

I. INTRODUCTION

In this lab experiment, we will carry out capacitance-voltage (CV) profiling on a reverse-biased Schottky barrier diode to determine the density of impurity dopants in its semiconductor layer as well as its built-in electric potential. In contrast to the more complicated dual-semiconductor structure of a \textit{pn} junction diode, a Schottky barrier diode consists of a single semiconductor layer in contact with a metallic layer. Due to the simplicity of its construction, the functioning of a Schottky barrier diode can be explained theoretically using only introductory electrodynamics and semiconductor concepts. As with all semiconductor devices, fabrication of a high-quality Schottky diode requires specialized expertise and expensive deposition systems. To avoid this hurdle, we use a commercially produced Schottky barrier diode in this project. Additionally, with an eye on containing the cost of the capacitance characterization system required to carry out this experiment, we describe two options for this setup that use low-cost op-amp circuitry and affordable computer-based instrumentation.

II. THEORY

A. Capacitance Profiling of Schottky Barrier

Consider a Schottky barrier of cross-sectional area \( A \), which consists of a metal layer in contact with a \textit{n}-type semiconductor (dielectric constant \( \epsilon \); for silicon, \( \epsilon = 11.7 \)), and define an \( x \)-axis whose origin is at the metal-semiconductor interface with its positive direction toward the semiconductor’s interior (Fig. 1). For the semiconducting material, we assume the following: (1) positively charged dopant atoms are incorporated in its lattice structure with a position-dependent volume number density ("doping density") \( \rho(x) \), (2) its temperature is high enough so that these dopant atoms are fully ionized, that is, their extra electrons have all been promoted into the semiconductor’s conduction band. These negative conduction electrons then perfectly compensate the dopant atom’s positive charge so that, in its bulk, the semiconductor is electrically neutral, and (3) at large \( x \), the semiconductor is connected
FIG. 1: Band bending in a Schottky barrier (cross-sectional area $A$) under bias of $-V_0$ creates a depletion region of width $W$ with space charge density $+e\rho$ due to ionized dopant atoms. When the reverse bias is increased by $dV_R$, an additional charge of $dQ = +e\rho(AdW)$ is created at the tail of the depletion region. Metal-semiconductor interface is at $x = 0$ and it is assumed each ionized dopant atom has charge of $+e$.

to external circuitry via an ohmic “back contact.”

We further assume that the type of metal is properly chosen so that when the two materials are joined, semiconductor conduction electrons transfer to the metal’s surface, leaving behind a positively charged layer of uncompensated dopant atoms (called the “depletion region”) in the volume of the semiconductor nearest the metal. This charge transfer takes place until the resulting space charge produces an electric potential $-V_{bi}$ at $x = 0$ (called the “built-in potential”), which prevents further flow of charge (because the Fermi levels of the two materials have been equalized).

If an externally applied voltage $-V_R$ (where $V_R \geq 0$ is called the “reverse bias”) is then
FIG. 2: Gauss’s Law applied to a Schottky barrier (cross-sectional area $A$) under bias of $-V_0 = -(V_R + V_{bi})$ to determine electric field $E$ at location $x$. By symmetry, the electric field $E$ is directed along $x$-axis. A (dashed) rectangular Gaussian surface is chosen with one face in the depletion region, where the space charge density is $+e\rho$; the other face is in neutral bulk region of the semiconductor, where the electric field $E = 0$. The total charge within the Gaussian surface is $dQ = +e\rho A(W - x)$. Metal-semiconductor interface is at $x = 0$.

applied at the metal contact so that the total potential at the metal-semiconductor interface is $-V_0 = -(V_R + V_{bi})$ and the total charge on the metal’s surface is $-Q$, movement of semiconductor conduction electrons away from the interface (and out the back contact at large $x$) will extend the depletion region to a width $W$. Beyond the depletion region, the semiconductor is neutral and the effect of $-Q$ is not felt (i.e., the electric field is zero here). This effect is called dielectric screening and $W$ is the screening length.

First, for simplicity, we assume a uniform doping density, that is, $\rho(x) = \rho$ (a constant), where each dopant atom has a single charge $+e$. If the cross-sectional dimensions of the Schottky barrier are much greater than $W$, by symmetry we can assume the electric field $E$ in the depletion region points in the (negative) $x$-direction. Then, using the rectangular Gaussian surface shown in Fig. 2 with one of its end caps in the neutral bulk region (where $E = 0$) and the other end cap located a distance $x$ from the metal-semiconductor interface,
Gauss’s law gives \( \epsilon E A = +e\rho A(W - x)/\epsilon_0 \). Then, for the electric potential \( V(x) \) as a function of the distance \( x \) into the depletion region, we have the two boundary conditions \( V(0) = -(V_R + V_{bi}) \) and \( V(W) = 0 \). Thus, from \( V(W) - V(0) = -\int_0^W E \cdot dx \), find

\[
V_R + V_{bi} = \frac{e\rho}{2\epsilon\epsilon_0} W^2
\]

(1)

and so the width of the depletion region required to screen out the applied bias \(-V_R\) is

\[
W = \sqrt{\frac{2\epsilon\epsilon_0(V_R + V_{bi})}{e\rho}}
\]

(2)

If the reverse bias \( V_R \) is increased by a small amount \( dV_R \), we find from Eq. (1) that \( dV_R = (e\rho/\epsilon\epsilon_0)W dW \), where \( dW \) is the increase in the depletion region’s width. This increase in the depletion region width is due to flow of conduction electrons at the edge of the depletion region into the semiconductor’s bulk (and out of the back contact), creating the extra space charge \( dQ = +e\rho(AdW) \) required to screen out the voltage change \(-dV_R\) at the metal-semiconductor interface. By definition, this process produces a capacitive response given by

\[
C \equiv \frac{dQ}{dV_R} = \frac{e\rho(AdW)}{(e\rho/\epsilon\epsilon_0)W dW} = \frac{\epsilon\epsilon_0 A}{W}
\]

(3)

or, using Eq.(2), the Schottky barrier’s capacitance as a function of applied reverse bias \( V_R \) is

\[
C = A \sqrt{\frac{\epsilon\epsilon_0 \rho}{2(V_R + V_{bi})}}
\]

(4)

This expression can be re-written as

\[
\frac{1}{C^2} = \frac{2}{A^2 \epsilon\epsilon_0 \rho} (V_R + V_{bi})
\]

(5)

Thus, for a Schottky barrier with uniform doping density, a plot of \( 1/C^2 \) versus \( V_R \) will yield a straight line with slope \( m = 2/A^2 \epsilon\epsilon_0 \rho \) and \( y \)-intercept \( b = 2V_{bi}/A^2 \epsilon\epsilon_0 \rho \). Then, the doping density and built-in potential are found from

\[
\rho = \frac{2}{A^2 \epsilon\epsilon_0 m}
\]

(6)

and

\[
V_{bi} = \frac{b}{m}
\]

(7)
The case of position-dependent doping density can be solved as follows: Starting with the following identity

\[
\frac{d}{dx} \left( x \frac{dV}{dx} \right) = \frac{dV}{dx} + x \frac{d^2V}{dx^2}
\]

(8)

and noting from Poisson’s equation that

\[
\frac{d^2V}{dx^2} = \frac{+e\rho(x)}{\varepsilon \varepsilon_0},
\]

(9)

we put Eq.(9) into (8). Then, integrating both sides of the resulting expression from \(x = 0\) to \(x = W\), yields

\[
V_R + V_{bi} = e \frac{\varepsilon \varepsilon_0}{\varepsilon_0} \int_0^W x \rho(x) dx
\]

(10)

If the reverse bias \(V_R\) is increased by a small amount \(dV_R\), the depletion region width will change by \(dW\), creating the extra space charge \(dQ = +e\rho(W)(AdW)\), where \(\rho(W)\) is the doping density at the edge of the depletion region when the reverse bias is \(V_R\). From Eq.(10)

\[
d(V_R + V_{bi}) = e \frac{\varepsilon_0}{\varepsilon_0} d \left( \int_0^W x \rho(x) dx \right)
\]

(11)

or

\[
dV_R = e \frac{\varepsilon_0}{\varepsilon_0} W \rho(W) dW
\]

(12)

Thus, the capacitive response is given by

\[
C \equiv \frac{dQ}{dV_R} = \frac{+e\rho(W)(AdW)}{(e/\varepsilon_0) W \rho(W) dW} = \frac{\varepsilon \varepsilon_0 A}{W}
\]

(13)

Re-writing this expression as \(1/C^2 = (W/\varepsilon_0 A)^2\) and then differentiating with respect to \(V_R\) gives

\[
\frac{d}{dV_R} \left( \frac{1}{C^2} \right) = \frac{1}{(\varepsilon_0 A)^2} 2W \frac{dW}{dV_R}
\]

(14)

or, using Eq.(12),

\[
\frac{d}{dV_R} \left( \frac{1}{C^2} \right) = \frac{1}{(\varepsilon_0 A)^2} 2W \left( \frac{\varepsilon_0}{eW \rho(W)} \right) = \frac{2}{\varepsilon \varepsilon_0 A^2 \rho(W)}
\]

(15)

This equation is called the “Profiler’s Equation” and can be used to characterize the spatial distribution of dopants in the semiconductor as follows: Starting with data for the
FIG. 3: Equivalent circuit of Schottky diode. Schottky barrier is modeled as capacitance $C$ in parallel with leakage resistance $R_L$. Semiconductor’s neutral bulk region (beyond the depletion region) contributes a series resistance $R_S$. For high-quality diode, impedance of $R_L$ is much greater than that of $C$ and $R_S$ is negligible. Thus the response of the diode is predominately due to $C$.

Schottky barrier’s capacitance $C$ as a function of applied reverse bias $V_R$, a plot of $1/C^2$ versus $V_R$ can be constructed. At each value of reverse bias $V_R$ on this plot, the slope $m = d(1/C^2)/dV_R$ can be determined and the associated value of capacitance $C$ noted. Then, each value of $V_R$ corresponds to probing the doping density at the distance $W$ from the metal-semiconductor interface given by [Eq.(13)]

$$W = \frac{\varepsilon \varepsilon_0 A}{C},$$

(16)

and, using Eq.(15), the doping density at this distance $W$ is given by

$$\rho(W) = \frac{2}{\varepsilon \varepsilon_0 A^2 m}$$

(17)

To carry out capacitance-voltage profiling of a Schottky barrier, a negative DC voltage $-V_R$ is applied to its metal contact with the back contact grounded, producing a space-charge region of width $W$ in the semiconductor. The barrier’s capacitance $C$ is then determined by adding a small AC modulation of amplitude $V_{ac}$ and angular frequency $\omega$ to the applied voltage. To account for a small leakage current through the barrier and the resistance
of the semiconductor’s neutral bulk region, the Schottky diode is modeled as the parallel combination of the capacitor $C$ and a leakage resistor $R_L$, in series with the series $R_S$. In most cases, the semiconductor doping density is large enough so that $R_S$ is negligible in comparison to the parallel combination of $C$ and $R_L$ and thus the equivalent circuit is that shown in Fig. 3. AC circuit analysis then predicts that the amplitude $I$ of the total AC current flowing in this circuit is

$$I = \frac{V_{ac}}{Z} = V_{ac}\left(\frac{1}{R_L} + i\omega C\right)$$

(18)

Hence, relative to the applied AC voltage, the current will have an in-phase component proportional to $1/R_L$ and a $90^\circ$ out of phase ("quadrature") component proportional to $\omega C$.

B. Lock-In Detection Algorithm

Assume that an experimental "in-phase signal" is the sinusoid $V_{sig}\sin(\omega_{sig}t)$, where $V_{sig}$ and $\omega_{sig}$ are the signal’s amplitude and angular frequency, respectively. If we construct a “reference” sinusoid $2\sin(\omega_{ref}t)$ of amplitude 2 and angular frequency $\omega_{sig}$, and then produce the product of the signal and reference, we obtain the following:

$$2V_{sig}\sin(\omega_{sig}t)\sin(\omega_{ref}t) = V_{sig}[\cos(\omega_{sig} - \omega_{ref})t - \cos(\omega_{sig} + \omega_{ref})t]$$

(19)

where we used the identity $\sin \alpha \sin \beta = 1/2[\cos(\alpha - \beta) - \cos(\alpha + \beta)]$. Thus, the multiplicative result is two AC sinusoids, each of amplitude $V_{sig}$, one with the “difference” frequency ($\omega_{sig} - \omega_{ref}$) and one with the “sum” frequency ($\omega_{sig} + \omega_{ref}$). Note that for the special case $\omega_{ref} = \omega_{sig}$, the difference-frequency sinusoid is the DC voltage $V_{sig}$. Thus, if an experimental waveform consists of a collections of component sinusoids of various frequencies, by multiplying this waveform by $2\sin(\omega_{ref}t)$ and then using a low-pass filter to find only the resultant DC value, one can determine the amplitude of the sinusoidal component within the experimental waveform whose frequency equals that of the reference.

In a similar way, if an experimental “quadrature signal” is $V_{sig}\cos(\omega_{sig}t)$, by multiplying by the “reference” $2\cos(\omega_{ref}t)$ and low-pass filtering for the resultant DC value, the value of the DC output is $V_{sig}$.  

7
III. EXPERIMENTAL SET-UP

Our goal is to demonstrate a low-cost, but accurate implementation of the capacitance profiling technique. We will first describe how the CV method would be carried out using research-grade stand-alone instrumentation in order to show how the technique works. With that background, we then show two inexpensive computer-based versions of this experiment, each based on an affordable USB-interfaced data acquisition device, that produce excellent results.

For each variant of the experiment, our sample is a commercially produced Schottky diode. Because the measured signal is proportional to the capacitor’s area, we chose a Schottky diode with a large-area metallic contact (Semiconix Semiconductor STPS20120D). The contact is composed of a TiW alloy. By stripped the epoxy encapsulation from one of these devices to expose the diode, a calibrated microscope was used to measure the square contact area to be $2.32 \text{ mm} \times 2.32 \text{ mm} = 5.38 \text{ mm}^2$. At zero applied bias, the capacitance of this diode is on the order of 1000 pF.

A. Research-Grade Implementation

A schematic diagram of a research-grade experimental setup is shown in Fig. 4. Here, a function generator (e.g., Agilent 33210A) applies an AC oscillation of frequency $f$ and (small) amplitude $V_{ac}$, along with a DC offset $-V_R$ to the Schottky diode metal contact. For our experiments, we will use $V_{ac} = 30 \text{ mV rms}$, $f = 1000 \text{ Hz}$, and $-V_R$ in the range from 0.0 to $-9.9 \text{ V}$. The other end of the diode is connected to a current preamplifier (e.g., DL Instruments 1211), which is a virtual electrical ground and converts the diode’s current $I$ (on the order of $\mu$A) to a voltage $V = \beta I$, where the proportionality constant $\beta$ is $10^6 \text{ V/A}$. For the diode we will use, these parameter result in a voltage on the order of $[V_{ac} \omega C] \times \beta = [(30 \text{ mV rms})2\pi(1000 \text{ Hz})(10^{-9} \text{ F})] \times 10^6 \text{ V/A} \approx 200 \text{ mV rms}$. This voltage is then read by a lock-in amplifier (e.g., Stanford Research System SR830). The function generator’s TTL sync output is used as the lock-in’s reference signal, with zero phase defined by the moment of the negative-going zero crossing of the AC oscillation (that is, the moment at which the reverse bias begins to increase). Since, at constant frequency, the lock-in’s quadrature voltage (which is proportional to the quadrature current) is proportional
to $C$ [Eq.(18)], a calibration capacitor $C_{cal}$ of known capacitance can be substituted in the circuit for the Schottky diode and the resultant quadrature voltage output $V_{cal}$ measured. Then, with the diode replaced back into the circuit, its capacitance $C_{diode}$ in response to a particular reverse bias is determined by measuring the quadrature voltage output $V_{diode}$ and using the following proportionality relation: $C_{diode}/C_{cal} = V_{diode}/V_{cal}$. A scan of capacitance as a function of reverse bias is typically taken under computer control and the resulting data analyzed via a $1/C^2$ versus $V_R$ plot to determine the semiconductor’s doping density via Eqs.(6) and (7) or Eqs. (16) and (17).

To account for small phase shifts due to other sources (e.g., cabling, amplifiers) than the capacitances of interest, a further refinement called “autophasing” can be included as follows: With the calibration capacitor replacing the Schottky diode in the circuit, record $V_{0x}$ and $V_{0y}$, i.e., the lock-in’s in-phase and quadrature readings for the known calibration capacitor, respectively. Then, assuming the calibration capacitor has a purely capacitive impedance (i.e., it has zero leakage current), these two readings determine a vector in the complex impedance plane that defines the direction of the sample’s capacitive response. With the diode back in the circuit, its in-phase and quadrature voltages $V_x$ and $V_y$, respectively, are measured. These two readings determine a vector describing the sample’s AC response in the complex impedance plane. By mathematically finding the component of the sample’s response along the purely capacitive direction (via a dot product), the following relation for the sample’s capacitance is obtained:

$$C_{diode} = \frac{(V_xV_{0x} + V_yV_{0y})}{V_{0x}^2 + V_{0y}^2} C_{cal}$$ (20)

Commercial research-grade lock-in amplifiers commonly offer autophasing with the push of a button.

B. Low-Cost Implementation

Our goal is to demonstrate that accurate CV profiling of a semiconductor can be carried out with a low-cost experimental set-up. We will describe two possible set-ups that can accomplish this goal. In each of these set-ups, the commercial current preamplifier is replaced by a simple current-to-voltage ($I$-to-$V$) op-amp circuit with a $10^6\,\Omega$ feedback resistor so that $\beta = 10^6\,\text{V/A}$. In addition, the required phase sensitive detection is carried out using a
FIG. 4: Research-grade implementation of Capacitance Profiling method using stand-alone instrumentation.

A computer-based lock-in amplifier consisting of an inexpensive data acquisition (DAQ) device and a LabVIEW software program. The central features of this computer-based lock-in are as follows: First, triggered by the negative-going transition of the function generator’s TTL sync output, the DAQ device acquires $N$ (a power of two) samples of the $I$-to-$V$ circuit’s voltage output. The sampling rate is chosen to be $f_{\text{sampling}} = N_{\text{point}} \times f$, where $N_{\text{point}}$ is the number of samples acquire during one reference cycle and $f$ is the reference frequency. A total of $N_{\text{cycle}}$ reference cycles are acquired so that the total number of acquired voltage samples is $N = N_{\text{point}} \times N_{\text{cycle}}$. Since the digitizing process is triggered at the our defined zero-phase angle, in software we create two copies of this acquired data waveform and multiply one copy by the reference $2 \sin(2\pi f)$ and the other copy by the reference $2 \cos(2\pi f)$. A fast Fourier transform is then taken of each of these arrays (hence the reason $N$ is chosen to be a power of two) and then the DC components of each picked out, resulting in the in-phase and
FIG. 5: LabVIEW code to carry out two-phase lock-in amplifier algorithm.

quadrature voltage amplitude at frequency $f$ in the original digitized waveform. Thus, the frequency bandwidth of our output signal is on the order of the FFT's frequency resolution $\Delta f = f_{\text{sampling}} / N$. We define the time constant of our lock-in algorithm to be $\tau \equiv 1 / \Delta f$, so $\tau = N / f_{\text{sampling}} = (N_{\text{point}} N_{\text{cycle}}) / (N_{\text{point}} f) = N_{\text{cycle}} / f$. Fig. 5 illustrates how this lock-in algorithm is programmed in LabVIEW.

We will describe how to carry out the above-described scheme using two different commonly used low-cost DAQ devices - the USB-6009 and the myDAQ. In each case, the manner in which the scheme is implemented must be adapted to the limitations of the DAQ device.

1. **Set-Up Using the USB-6009**

The USB-6009 device performs 14-bit analog-to-digital conversions of an incoming signal at rates up to 48,000 Samples per second (S/s). Each $N$ sample acquisition can be hardware triggered by a TTL signal. The device’s programmable-gain amplifier allows for eight possible input voltage ranges over which to spread the 14-bit resolution. Since our input signal is on the order of a few hundred millivolts, we choose the (device’s most sensitive) $\pm 1$ V range. Additionally, given the 48 kS/s maximum sampling rate and that fact that we need the number of samples per cycle (i.e., $N_{\text{point}}$) to be a power of two, we chose our reference frequency to be 1000 Hz. Then, $N_{\text{point}}$ can be 32, the minimum value we feel necessary to properly describe the 1000 Hz signal. Finally, this DAQ device possesses only modest digital-to-analog conversion capabilities. With a maximum analog output update rate of
FIG. 6: Low-cost implementation of Capacitance Profiling using USB-6009 DAQ device. Op-amp circuit serves as current preamplifier and lock-in algorithm carried out using hardware-triggered DAQ device and LabVIEW software. Because DAQ device has minimal waveform generation capabilities, stand-alone computer-interfaced function generator (e.g., Agilent 33210A) is used.

only 150 Hz, the USB-6009 cannot produce the reference signal we require for our experiment. Hence, we retain the stand-alone function generator (e.g., USB-interfaced Agilent 33210A) for this set-up as shown in Fig. 6.

With \( f = 1000 \) Hz, choose \( N_{\text{point}} = 32 \) and \( N_{\text{cycle}} = 512 \). Then, \( f_{\text{sampling}} = 32,000 \) S/s, \( N = 16,384 \) (\( = 2^{14} \)), and \( \tau = 0.51 \)s. Use a 1 nF capacitor as the calibration capacitor (if available, accurately determine its value \( C_{\text{cal}} \) with an LCR meter). Using these parameters, acquire room-temperature capacitance-voltage data with reverse bias voltages ranging from 0.0 to 9.9 V in increments of 0.1 V.
FIG. 7: Low-cost implementation of Capacitance Profiling using myDAQ DAQ device. Op-amp circuit serves as current preamplifier and lock-in algorithm carried out using software-triggered DAQ device and LabVIEW software. Waveform generation function of myDAQ device is used to create modulated reverse bias; op-amp low-pass filter suppresses digitizing steps on small-amplitude AC modulation.

2. **Set-Up Using the myDAQ**

The myDAQ device performs 16-bit analog-to-digital conversions of an incoming signal at rates up to 200,000 S/s. The device’s programmable-gain amplifier allows for two possible input voltage ranges; we choose the (device’s most sensitive) ±2 V range. However, the device offers no hardware triggering capability for these digitizing operations. Thus, the triggering for the voltage acquisitions must be done in software. Finally, this DAQ device can also perform digital-to-analog conversions at rates up to 200,000 S/s on two analog output (AO) channels. We use these two AO channels to produce our required modulated
FIG. 8: Low-cost implementation of Capacitance Profiling using myDAQ DAQ device. Op-amp circuit serves as current preamplifier and lock-in algorithm carried out using software-triggered DAQ device and LabVIEW software. Waveform generation function of myDAQ device is used to create modulated reverse bias; op-amp low-pass filter suppresses digitizing steps on small-amplitude AC modulation.

bias voltage as well as a digital reference signal whose transitions are in-phase with the bias voltage’s AC modulation. As shown in Fig. 8, the square-wave reference signal generated by one of the analog output channels is directly connected to, and read, by one of the analog input channels. The moment at which a transition of this square occurs is determined by searching the acquired waveform in software, enabling lock-in detection. Fig. 9 illustrates how software triggering is carried out in LabVIEW.

With \( f = 1000 \text{ Hz} \), choose \( N_{\text{point}} = 128 \) and \( N_{\text{cycle}} = 512 \). Then, \( f_{\text{sampling}} = 128,000 \text{ S/s} \), \( N = 65,536 \) \( (= 2^{16}) \), and \( \tau = 0.51 \text{s} \). Using these parameters, acquire room-temperature capacitance-voltage data with reverse bias voltages ranging from 0.0 to 9.9 V in increments
FIG. 9: LabVIEW code to carry out software analog triggering.

of 0.1 V.

IV. DATA ANALYSIS

Plot $1/C^2$ versus $V_R$. If your plot yields a straight line, that indicates that the diode's doping density is constant over the spatial region profiled. Using Eqs.(6 and 7), determine the doping density (units of dopants/cm$^3$) in this region and the diode's built-in potential (units of V).

Additionally, use Eqs.(16) and (17) to produce a plot of $\rho(x)$ versus $W$, i.e., the spatial variation of the doping density as a function of distance from the metal-semiconductor interface.
Sample Data

Data from USB-6009 Implementation

Using Eqs. (6) and (7) with $A = 5.38 \text{ mm}^2$ gives $\rho = 2.6 \times 10^{15} \text{ dopants/cm}^3$ and $V_{bi} = 0.61 \text{ V}$.

Using Eqs. (16) and (17) gives
Data from myDAQ Implementation:

Using Eqs. (6) and (7) with $A = 5.38 \text{ mm}^2$ gives $\rho = 2.7 \times 10^{15} \text{ dopants/cm}^3$ and $V_{bi} = 0.63 \text{ V}$.