

# Using Digilent's Basys3 FPGA board with LabVIEW for single-photon counting

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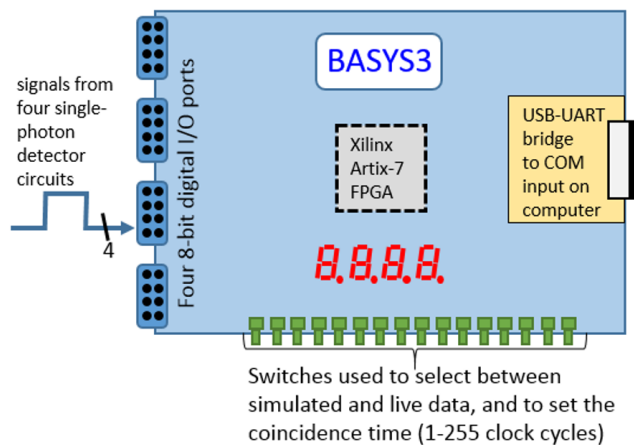
**Abstract:** The Basys3 board produced by Digilent and featuring the Artix-7 FPGA (Field Programmable Gate Array) promises to provide the fast electronic signal processing required to perform single-photon counting. The Basys3 compares favorably in terms of cost, speed, and convenience to the Altera-brand FPGA's that have been described by other authors. LabVIEW provides a flexible and convenient way to control the FPGA board and to graphically represent what is happening with the various counts in real time. Details about how to use the Basys3 board and information about how to interface the board with LabVIEW in the context of a single-photon counting experiment are described.

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## I. INTRODUCTION

Single-photon detectors are now available at a cost that is significantly lower than similar research-grade detectors. This is due in part to the advocacy of ALPhA, the Advanced Laboratory Physics Association [1], and puts quantitative measurements of a variety of quantum phenomena (quantum erasers, tests of Bell's inequalities, and other manifestations of quantum entanglement) within the reach of students in an undergraduate advanced lab course. But in order to fully realize the capabilities of these new detectors, fast and flexible electronic signal processing is necessary. In addition, given the time and cost constraints of an undergraduate course, an inexpensive and easy-to-use solution is especially important.

Several investigators have used FPGAs for single-photon counting, coincidence, and correlation experiments [2-4]. This is because FPGAs are easy to use, inexpensive, and have relatively fast clock speeds (50 MHz and up). In addition, the flexible architecture of FPGAs permits designs with truly parallel processing. This allows multiple calculations to execute on a single clock cycle.



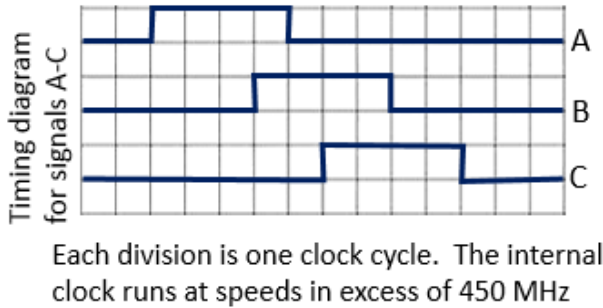
**FIG 1.** Schematic of the Basys3 board showing the digital I/O ports, switches, and USB-UART bridge used for coincidence counting.

## II. EXPERIMENTAL PROCEDURE

Unlike the previously mentioned experiments, this project was built around Digilent's Basys3 board as shown in Fig. 1. The board is an inexpensive entry-level board that contains Xilinx's Artix-7 FPGA, 16 switches, four 7-segment displays, 16 LEDs, 5 buttons, four 8-bit digital expansion input/output (I/O) ports, and a build-in USB-UART bridge for easy computer interfacing. The board is available from [www.digilent.com](http://www.digilent.com) for \$79 (academic price). This is especially impressive considering that digikey.com offers a comparable bare version of the Artix-7 (484GBA) for \$80.57. The Basys3 is programmed using Vivado Design Suite [5].

Although the on-board master clock runs at 100 MHz the clock can be fractionally divided using a mixed mode clock manager (MMCM) to achieve speeds exceeding 450 MHz. A clocking wizard is available in the intellectual property (IP) catalog within Vivado that will generate customized code according to user specifications. The coincidence counting circuit was designed to receive a 3.3 V digital signal from each of four single-photon detector circuits (A -D). While running, the FPGA continually records all of the possible single counts and coincidences, see Fig. 2. Each count is housed in a separate register on the FPGA. The values from all of these registers are sent to the computer every second using the USB-UART bridge which has an FT2232HQ chip from FTDI (Future Technology Devices International Limited) with a FIFO buffer (first in, first out) to handle the data flow.

The toggle switches on the board are used to change a variety of system parameters. One switch determines whether the FPGA uses the signals from the detectors or uses an internally generated signal that is useful for debugging purposes. Eight of the switches determine the coincidence time in clock cycles (1-255). Four switches determine which of the counting registers is displayed on the LEDs.



Coincidence between detectors?			
AB	AC	BC	ABC
✓	✗	✓	✗

**FIG 2.** Timing diagram showing the signals that are generated within the FPGA upon triggering from three of the four single-photon detectors (A – C). In this example the coincidence time is set to 4 clock cycles (represented as grid divisions). This event would increment the counting registers A, B, & C since those three detectors have fired. This event would also increment the coincidence counters for registers AB and BC since there is overlap between each of the indicated signals. However the coincidence count would *not* be incremented for registers AC or ABC since A & C are not coincident within 4 clock cycles.

A LabVIEW Virtual Instrument (VI) was created to control the experiment, to provide real-time feedback about count rates, and to automatically save the data to disk. Data from the USB/UART bridge was accessed using the computer’s COM port. A detail from the VI’s block diagram and front panel are shown in figures 3 & 4. The toggle switches (A-D) allow the user to display one of 16 possible counting rates. This includes all 4 detector counts (A-D) and all 6 double coincidences (AB, AC, AD, BC, BD, CD), all 4 triple coincidences (ABC, ABD, ACD, BCD), the ABCD coincidence when all the detectors fire within the same coincidence window and the null case where none fires. In the example shown in figure 4, the buttons A, C, & D appear in color indicating that the ACD coincidence is being displayed. The dial and live-scrolling chart are useful for monitoring the experiment and for aligning the optics. The VI front panel contains four of these blocks allowing the user to monitor four different counts at once. Although only four counts can be displayed at a time, the VI writes all 16 counts into a spreadsheet.

### III. RESULTS AND DISCUSSION

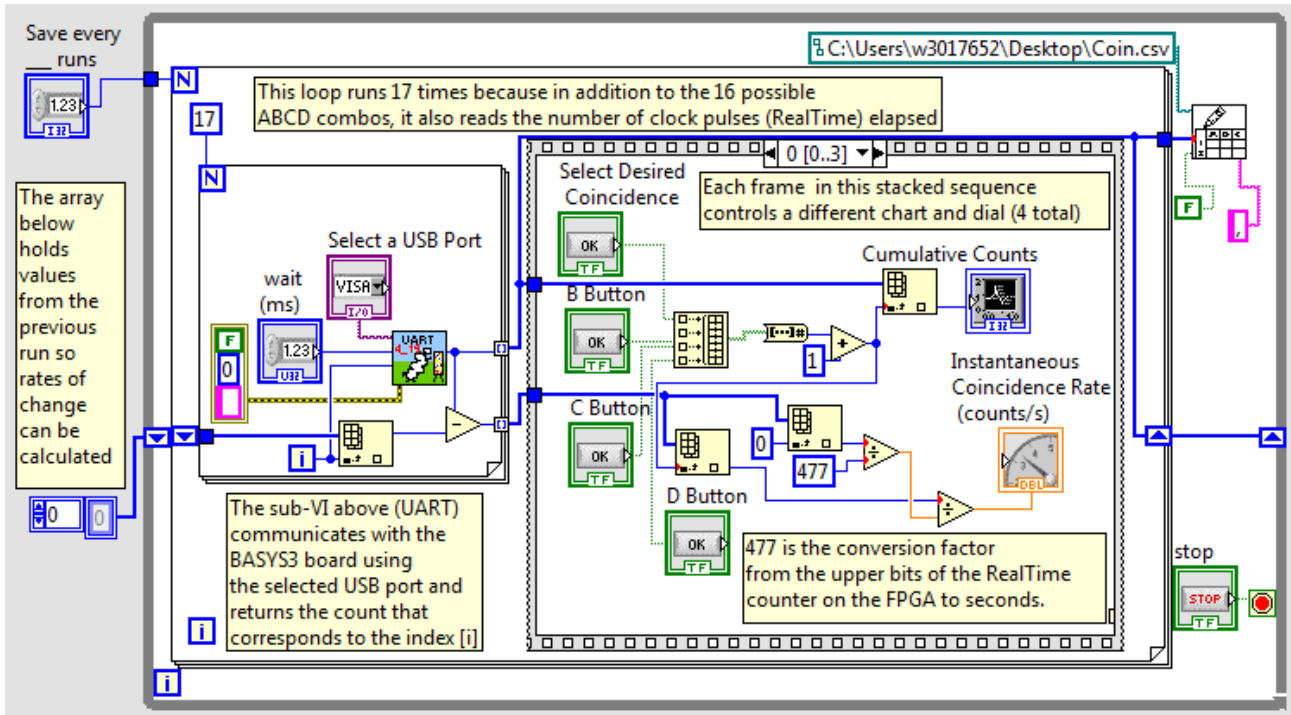
The electronics described here have been built and tested with both real data from the Excelitas detectors [1] as well as with simulated data. i.e., data generated by the FPGA for

troubleshooting purposes. In these tests the FPGA has performed reliably and the LabVIEW interface has provided an intuitive control system. It should be noted, however, that this paper represents a preliminary report on the progress of the project and as such the circuits have not yet been tested in the context of a complete coincidence experiment.

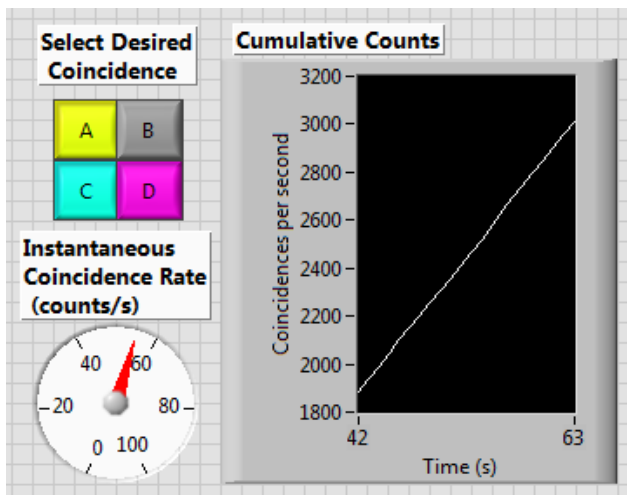
It’s worth noting that this approach uses a different make of FPGA than the other experiments mentioned. Byung Kwon Park, *et al.* used the Altera DE0-Nano Development and Education Board with an Altera Cyclone IV. It has a maximum frequency of 163 MHz and requires an external USB-to-Serial Board (the FT232H from ROVITECK). Benjamin Gamari, *et al.*, selected the KNJN Xylo EM FPGA development board which includes an Altera Cyclone II FPGA. The board was modified with a 32 MHz external crystal which was then multiplied to achieve a 128 MHz clock. David Branning, *et al.*, used an Altera Acex 1K FPGA running at 50 MHz for communication but built the logic out of F-series TTL (transistor transistor Logic) chips.

Several features make the Digilent board (with the Xilinx Artix-7 FPGA) a reasonable alternative to the Altera FPGAs: 1) the fact that the Digilent board has a built-in USB-UART bridge 2) the fact that the Artix-7 has internal clock speeds exceeding 450 MHz and 3) that the MMCM required to achieve these speeds is configurable by way of a clock wizard that is freely available in the IP catalog within the Vivado environment 4) finally, the fact that Xilinx controls half of the FPGA market share makes the Digilent solution convenient for those already familiar with Xilinx products as well as for students who will use Xilinx products in future careers.

While having a faster clock increases the time resolution of the experiment generally, it may have another benefit as well. Output pulses from single-photon counting modules (SPCMs) can be quite short, typically 6 ns – 15 ns [6, 7]. If the clock on the FPGA is too slow then there will be a chance that it won’t register the data during the period that the output pulse is active and the count will be lost. For output signals of 15 ns a clock just faster than 67 MHz is sufficient. For output signals that are 6 ns long the clock must be faster than 167 MHz in order to catch all of the counts. In order to make a slower clock function correctly it’s possible to add circuitry that will extend the pulse time. Having a faster clock eliminates the need for this extra circuitry.



**FIG. 3** Block diagram of the VI that communicates with the Basys3 board. In addition to displaying the cumulative counts and instantaneous count rate for four selected counts, the VI writes the total number of clock pulses measured by the board (RealTime) and all 16 possible detector counts and coincidence counts to a spreadsheet.



**FIG. 4** A detail from the LabVIEW front panel. Although the FPGA records ALL 4 detector counts (A-D) and all 11 possible coincidences the LabVIEW GUI (graphical user interface) allows the user to easily select which coincidence to display. In this case buttons A, C, & D have been toggled “ON” (as indicated by their colors) so the count rate shown corresponds to the coincidence between detectors A, C, & D. The data shown was simulated by the FPGA running in debug mode.

## IV. CONCLUSIONS

The Basys3 board by Digilent can provide an inexpensive and convenient way to access the speed and computing power of the Artix-7 FPGA. Controlling the board with a GUI (graphical user interface) like a LabVIEW VI, overcomes the limited I/O options available on the board to produce a control console that is easy to read, easy to understand and easy to adjust. This makes it an ideal option for coincidence counting in the context of undergraduate courses.

## ACKNOWLEDGEMENTS

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