Pulse Width Modulation & FPGA

Sigma Delta Pulse Width Modulated Sine Wave

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PWM Theory

\[ \langle V_{out} \rangle = \frac{\tau_{on}}{\tau_{swc}} V_{on} \]
PWM Circuit Components

Switch

$V_{on}$

$V_{out}$

$R$

$C$

PWM_out

$x_{in}$

clk_in

Switch Control Algorithm, i.e., PWM Algorithm
Simple PWM Control Algorithm

- An n-bit counter continuously increments from 0 to its maximum value, i.e., $2^n-1$ and then repeats the cycle.
- Range of input value $x_{in}$: $0 \leq x_{in} \leq 2^n-1$

```plaintext
if ( counter < x_in )
    PWM_out <= 1;
else
    PWM_out <= 0;
```

```
counter <= counter+1;
```
Verilog Implementation of Simple 8 Bit PWM Algorithm

module SimplePWM(clk_in, x_in, PWM_out);

input clk_in;       //clock for counter
input [7:0] x_in;   //control value that defines pulse width
output reg PWM_out = 1;  //PWM signal out

reg [7:0] counter = 0;

always@ (posedge clk_in )begin
  if ( counter < x_in )
    PWM_out <= 1;
  else
    PWM_out <= 0;
  counter <= counter+1;
end
endmodule
A2D Key Concepts: Resolution / Sensitivity

• Resolution of an n-bit PWM A2D is: $V_{on} / 2^n$

• (Hypothetical) Resolution for our BASYS board PWM A2D with $V_{on} = 5$ Volts would be:

<table>
<thead>
<tr>
<th>bits</th>
<th>Resolution (Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>1.9E-02</td>
</tr>
<tr>
<td>16</td>
<td>7.6E-05</td>
</tr>
<tr>
<td>32</td>
<td>1.2E-09</td>
</tr>
<tr>
<td>64</td>
<td>2.7E-19</td>
</tr>
</tbody>
</table>
A2D Key Concepts: Conversion Time

• It takes at least one complete counter cycle to average $V_{out}$. For a counter running at $f_o$, this corresponds to: $2^n/f_o$.

• (Optimal) Conversion Time for our BASYS board PWM A2D with $f_o = 25$ MHz:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Resolution (Volts)</th>
<th>Conversion Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>1.9E-02</td>
<td>10.2 usec</td>
</tr>
<tr>
<td>16</td>
<td>7.6E-05</td>
<td>2.6 msec</td>
</tr>
<tr>
<td>32</td>
<td>1.2E-09</td>
<td>2.8 min</td>
</tr>
<tr>
<td>64</td>
<td>2.7E-19</td>
<td>23000 years</td>
</tr>
</tbody>
</table>
Sigma Delta Concepts

Though $V_{\text{out}}(t)$ is different in each of these timing diagrams, $<V_{\text{out}}>$ remains identical.
Sigma Delta PWM Algorithm

if (Sigma >= Delta)
{
Sigma = (Sigma - Delta) + x_in;
Out = 1;
}
else
{
Sigma = Sigma + x_in;
Out = 0;
}
PWM Application: Music Player
Conclusions about PWM

• Pulse Width Modulation can be used to create an analog signal from a digital signal.

• Allows the reduction of a DC signal while being much more energy efficient than, for example, a passive voltage divider.

• Sigma Delta algorithm can also be used for voltage to frequency conversion.
Educational Goals

• The PWM exercises expose students to basic digital concepts such as clocks and counters.
• They are easily implemented with an FPGA and thereby exposes students with this ubiquitous electronic component.
• Familiarizes them with digital-to-analog converters and the basic concepts of resolution and conversion time.
• The exercise can be extended by turning it into an analog-to-digital converter using successive approximation and a state machine.